

4Mbit, 512KX8 CMOS S-RAM (Monolithic)

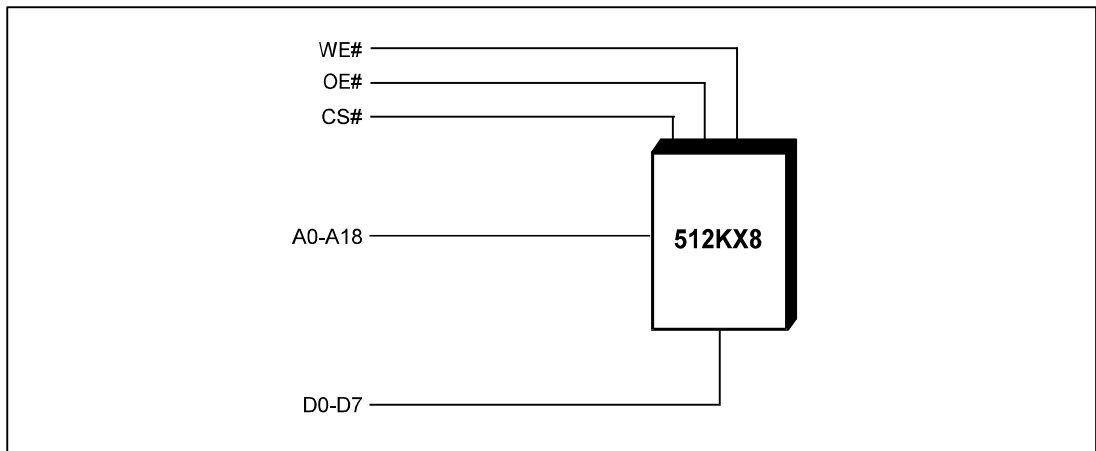
Features

- Access Times: 17, 20ns
- Package Options:
 - 32-Pin Ceramic DIP
JEDEC Approved Pinout
 - 36-Lead Ceramic SOJ
JEDEC Approved Revolutionary Pinout
- Industrial and Military Screening
- TTL Compatible Input/Output
- Single 5V ($\pm 10\%$) Power
- Data Retention
(Low Power Version Only)

Product Description

The MES5128 is a Monolithic 4 Megabit Static Ram. The module is organized as 512Kx8 and packed in a multilayer High Temperature cofired ceramic package, designed for better speed performance. These modules are available in 20ns and 17ns.

Block Diagram



Pin Names

Pin Name	Pin Function
A0÷A18	Address Inputs
D0÷D7	Data Inputs/Outputs
CS#	Chip Select
WE#	Write Enable
OE#	Output Enable
GND	Ground
Vcc	Power (+5V ±10%)
NC	No Connection

Truth Table (H=V_{IH} L=V_{IL} X=Don't Care)

OE#	WE#	CS#	I/O	Mode
X	X	H	Hi-Z	Standby
L	H	L	Dout	Read
X	L	L	Din	Write
H	H	L	Hi-Z	Out Disable

Note: # Symbol means Active Low Signal

Pin Configurations (Top View)

DIP (D)

1	● A18	Vcc ●	32
2	● A16	A15 ●	31
3	● A14	A17 ●	30
4	● A12	WE# ●	29
5	● A7	A13 ●	28
6	● A6	A8 ●	27
7	● A5	A9 ●	26
8	● A4	A11 ●	25
9	● A3	OE# ●	24
10	● A2	A10 ●	23
11	● A1	CS# ●	22
12	● A0	D7 ●	21
13	● D0	D6 ●	20
14	● D1	D5 ●	19
15	● D2	D4 ●	18
16	● GND	D3 ●	17

CSOJ (J)

1	A0	N.C	36
2	A1	A18	35
3	A2	A17	34
4	A3	A16	33
5	A4	A15	32
6	CS#	OE#	31
7	D0	D7	30
8	D1	D6	29
9	Vcc	GND	28
10	GND	Vcc	27
11	D2	D5	26
12	D3	D4	25
13	WE#	A14	24
14	A5	A13	23
15	A6	A12	22
16	A7	A11	21
17	A8	A10	20
18	A9	N.C	19

Absolute Maximum Ratings

Item	Rating
Supply Voltage Relative to GND	-0.5V to +7.0V
Voltage on Any Pin Relative to GND	-0.5V to V _{CC} +0.5V
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating (Military) Temperature (Industrial)	T _A	-55	+125	°C
		-40	+85	°C

Capacitance (T_A = +25°C, V_{IN} = 0V, f = 1.0 MHz)

Description	Symbol	Limits		Unit
		Min	Max	
Input Capacitance	C _{IN}		20	pF
Output Capacitance	C _{OUT}		20	pF

These parameters are guaranteed, but not tested.

DC Characteristics ($V_{CC} = 5V$)

Parameter	Symbol	Min	Max	Units
Input Leakage Current	$I_{LI}^{(1)}$	-2	2	μA
Output Leakage Current	$I_{LO}^{(2)}$	-2	2	μA
Output Low Voltage	$V_{OL}^{(3)}$		0.4	V
Output High Voltage	$V_{OH}^{(4)}$	2.4		V
Standby Supply Current	$I_{SB}^{(5)}$	17ns *	20	mA
		20ns	20	
Dynamic Operating Current	$I_{CC}^{(6)}$	17ns *	100	mA
		20ns	100	

(*) - Contact factory for information

Notes:

- (1) $V_{CC} = \text{Max}$, $V_{IO} = V_{CC}$ to GND.
- (2) $V_{IO} = V_{CC}$ to GND, $CS\# \geq V_{IH}$, $OE\# \geq V_{IH}$.
- (3) $V_{CC} = \text{Min}$, $I_{OL} = +8mA$.
- (4) $V_{CC} = \text{Min}$, $I_{OH} = -4mA$.
- (5) $CS\# = V_{IH}$, $OE\# = V_{IH}$, $V_{CC} = \text{Max}$, $f = 5MHz$.
- (6) $V_{CC} = \text{Max}$, $CS\# = V_{IL}$, $OE\# = V_{IH}$, $f = 5MHz$.

AC Characteristics

Write Cycle

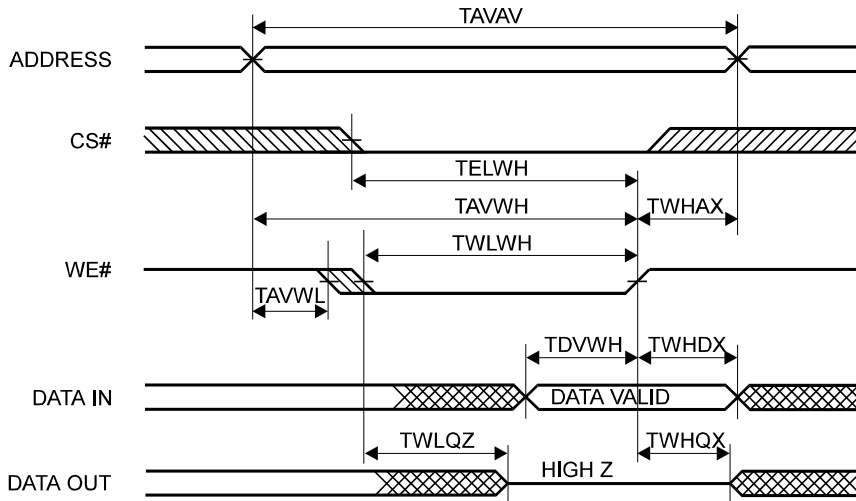
Parameter	Symbol	17ns	20ns	Limits	Unit
Write Cycle Time	TAVAV	17	20	min	ns
Address Set-up Time	TAVWL	0	0	min	ns
Address Valid to End of Write	TAVWH	14	14	min	ns
Data Valid to End of Write	TDVWH	9	9	min	ns
Chip Select Low to End of Write	TELWH	13	13	min	ns
Write Pulse Width	TWLWH	13	13	min	ns
Address Hold from Write End	TWHAX	0	0	min	ns
Data Hold Time	TWHDX	0	0	min	ns
Write Enable Low to High Z	TWLQZ *	8	8	max	ns
Output Active from End of Write	TWHQX *	0	0	min	ns

Read Cycle

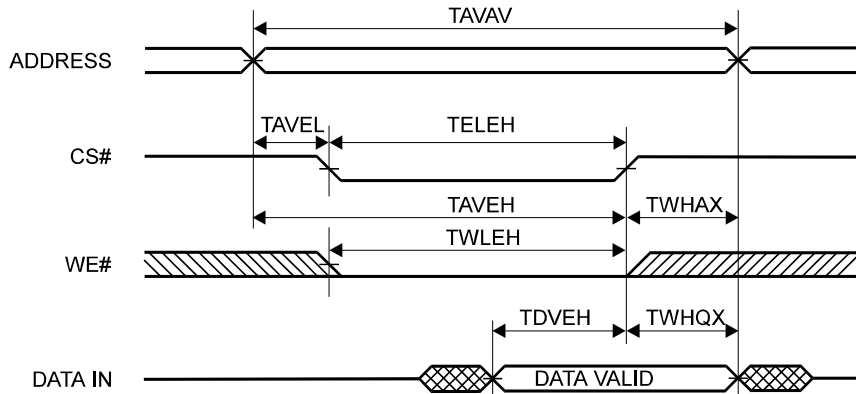
Parameter	Symbol	17ns	20ns	Limits	Unit
Read Cycle Time	TAVAV	17	20	min	ns
Address Access Time	TAVQV	17	20	max	ns
Output Hold from Addr. Change	TAVQX	4	4	min	ns
Chip Select Access Time	TELQV	17	20	max	ns
Output Enable to Output Valid	TGLQV	9	10	max	ns
Chip Select to Output in Low Z	TELQX *	3	3	min	ns
Chip Disable to Output in High Z	TEHQZ *	10	10	max	ns
Output Enable to Output in Low Z	TGLQX *	0	0	min	ns
Output Disable to Output in High Z	TGHQZ *	10	10	max	ns

(*) - Parameter is guaranteed, but not tested.

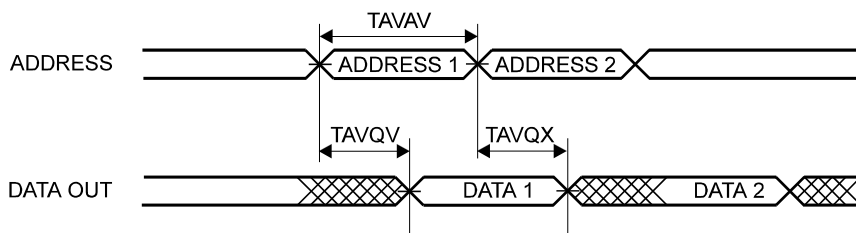
Write Cycle 1: WE# Controlled (OE# = V_{IH})



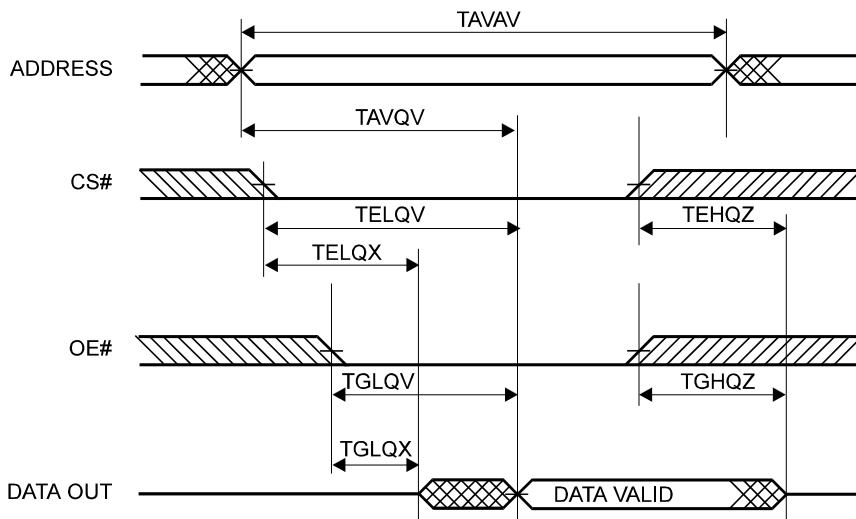
Write Cycle 2: CE# Controlled (OE# = V_{IH})



Read Cycle 1 (CS# = OE# = VIL, WE# = VIH)



Read Cycle 2 (WE# = VIH)



AC Test Conditions

Item	Conditions
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load:	25ns to 70ns 85ns and up
	1 TTL Load, CL=30pF 1 TTL Load, CL=100pF

Note: For TWHQX, TWLQZ, TEHQZ, TELQX, TGHQZ and TGLQX CL = 5pF

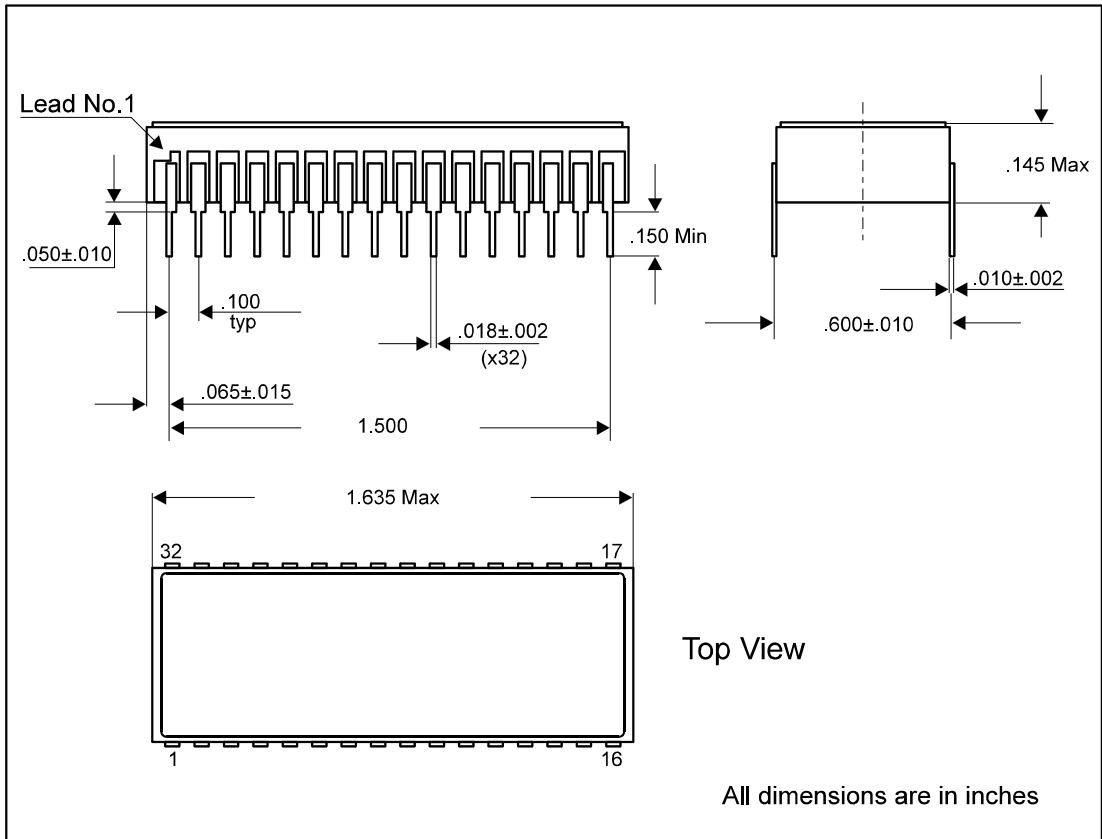
Data Retention Characteristics (Over Operating Temp Range) For Low Power Version Only ⁽¹⁾

Test Conditions: GND = 0V, V_{CC} = 3V, CE# ≥ V_{CC}-0.2V, V_{IH} ≥ V_{CC} - 0.2V, V_{IL} ≤ 0.2V.

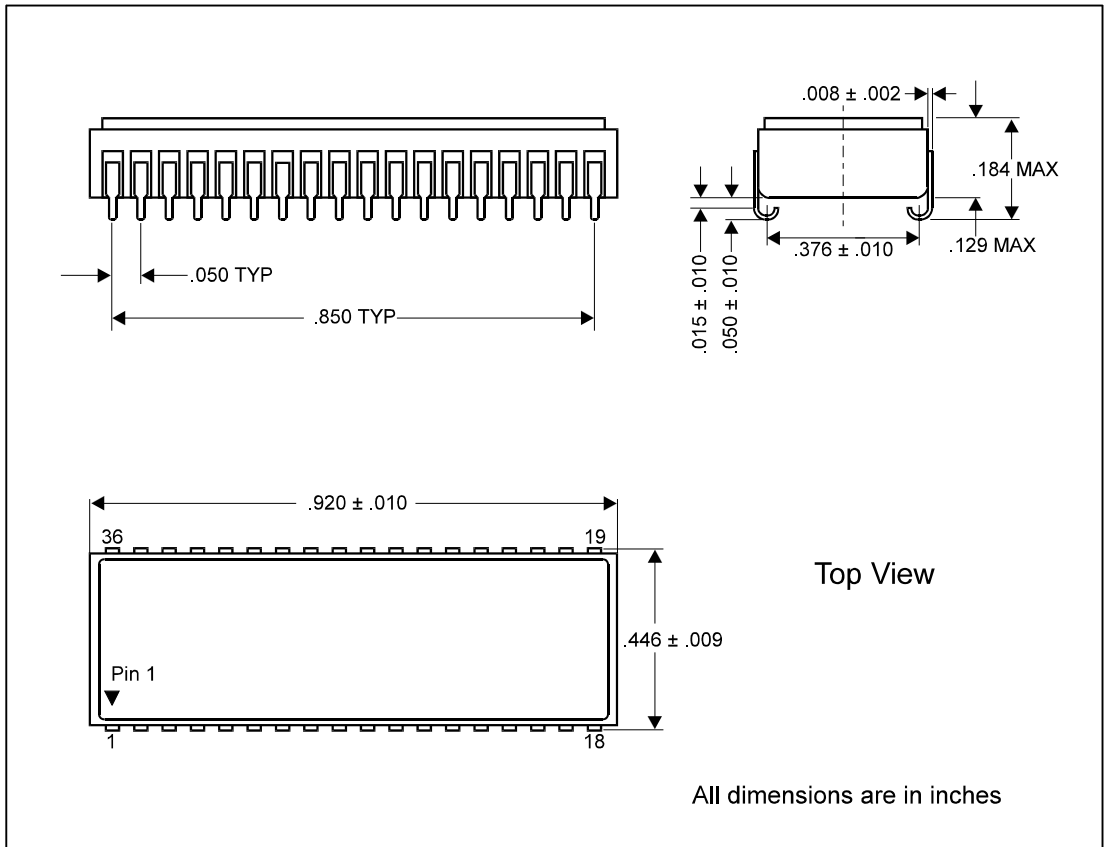
Characteristic	Symbol	Min	Typ.	Max	Unit
V _{CC} for Data Retention	V _{DR}	2			V
D.R Quiescent Current	I _{CCDR}		500 ⁽²⁾	2000 ⁽²⁾	μA

(1) Contact factory (2) Lower D.R Currents are available upon request

Outline Drawing for 32-Pin Ceramic DIP (D)



Outline Drawing for 36-Lead Ceramic SOJ (J)

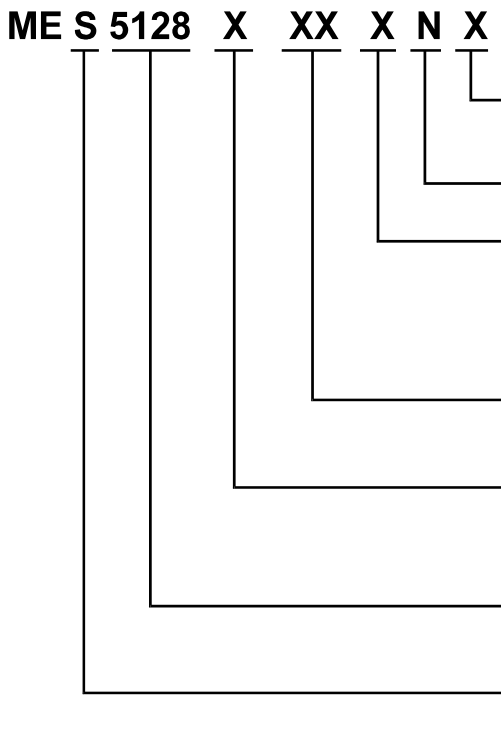


Ordering Information (Standard Military Screened Products*)

<i>Model Number</i>	<i>Speed</i>	<i>Package</i>
MES5128D17MNL	17ns	CDIP32
MES5128D20MNL	20ns	CDIP32
MES5128J17MNL	17ns	CSOJ36
MES5128J20MNL	20ns	CSOJ36

(*) - Contact Elisra for additional designs

Part Number Breakdown



Low Power Option

L = Data Retention

Monolithic

Screening Options

M = Military Full Screen

E = Extended Temp Range (- 55°C to + 125°C)

I = Industrial Grade (- 40°C to + 85°C)

Speed Options

Access Time (tAA) in ns

Package Options

D = 32-Pin Ceramic DIP

J = 36-Lead Ceramic SOJ

Organization

512KX8

Memory Type

Static Ram