

## 2Mbit, 256KX8 CMOS S-RAM MODULE

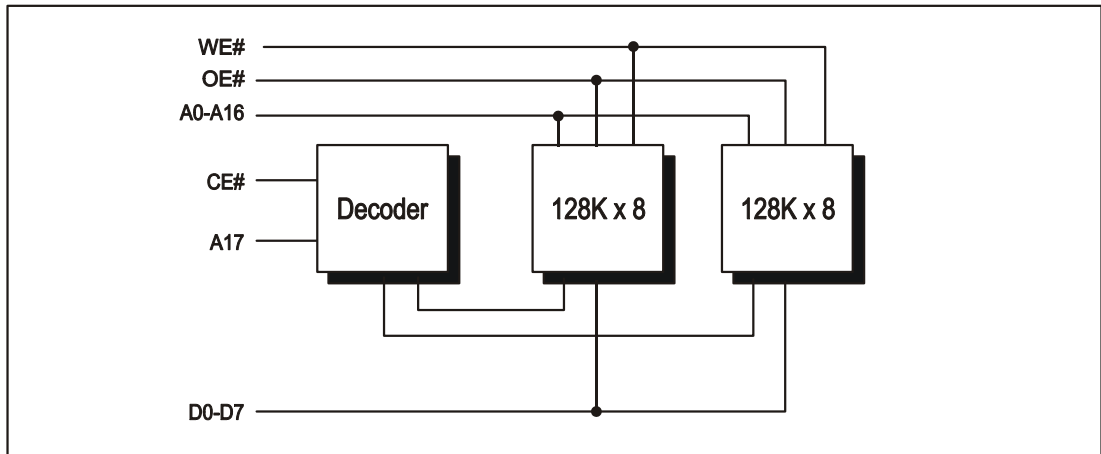
### Features

- Access Times: 25, 35 and 45ns
- 32 Pin DIP, JEDEC Standard Pin Configuration
- Industrial and Military Screening
- Data Retention (Low Power Version Only)
- TTL Compatible Input/Output
- Fully Static, No Clocks
- Single 5V ( $\pm 10\%$ ) Power

### Product Description

The MES2568D is a Family of 2 Megabit Static Ram modules organized as 256Kx8. Each module is constructed from two 128Kx8 Static Rams. The 32-DIP package is a multilayered High Temperature cofired ceramic package designed for high speed and better ground bounce. These modules are available in 25 to 45 versions.

### Block Diagram



**Pin Names**

| Pin Name | Pin Function        |
|----------|---------------------|
| A0÷A17   | Address Inputs      |
| DQ0÷DQ7  | Data Inputs/Outputs |
| CE#      | Chip Enable         |
| WE#      | Write Enable        |
| OE#      | Output Enable       |
| GND      | Ground              |
| Vcc      | Power (+5V ±10%)    |
| NC       | No Connection       |

**Truth Table** (H=V<sub>IH</sub> L=V<sub>IL</sub> X=Don't Care)

| OE# | WE# | CS# | I/O  | Mode        |
|-----|-----|-----|------|-------------|
| X   | X   | H   | Hi-Z | Standby     |
| L   | H   | L   | Dout | Read        |
| X   | L   | L   | Din  | Write       |
| H   | H   | L   | Hi-Z | Out Disable |

**Note:** # Symbol means Active Low Signal

**Pin Configuration** (Top View)

|    |       |       |    |
|----|-------|-------|----|
| 1  | ● NC  | Vcc ● | 32 |
| 2  | ● A16 | A15 ● | 31 |
| 3  | ● A14 | A17 ● | 30 |
| 4  | ● A12 | WE# ● | 29 |
| 5  | ● A7  | A13 ● | 28 |
| 6  | ● A6  | A8 ●  | 27 |
| 7  | ● A5  | A9 ●  | 26 |
| 8  | ● A4  | A11 ● | 25 |
| 9  | ● A3  | OE# ● | 24 |
| 10 | ● A2  | A10 ● | 23 |
| 11 | ● A1  | CE# ● | 22 |
| 12 | ● A0  | D7 ●  | 21 |
| 13 | ● D0  | D6 ●  | 20 |
| 14 | ● D1  | D5 ●  | 19 |
| 15 | ● D2  | D4 ●  | 18 |
| 16 | ● GND | D3 ●  | 17 |

## Absolute Maximum Ratings

| Item                               | Rating             |
|------------------------------------|--------------------|
| Supply Voltage Relative to GND     | -0.5V to +7.0V     |
| Voltage on any Pin Relative to GND | -0.5V to Vcc +0.5V |
| Operating Temperature              | -55°C to +125°C    |
| Storage Temperature                | -65°C to +150°C    |

## Recommended Operating Conditions

| Parameter                          | Symbol          | Min  | Max      | Unit |
|------------------------------------|-----------------|------|----------|------|
| Supply Voltage                     | Vcc             | 4.5  | 5.5      | V    |
| Input High Voltage                 | V <sub>IH</sub> | 2.2  | Vcc +0.3 | V    |
| Input Low Voltage                  | V <sub>IL</sub> | -0.5 | +0.8     | V    |
| Operating Temperature (Military)   | T <sub>A</sub>  | -55  | +125     | °C   |
| Operating Temperature (Industrial) |                 | -40  | +85      | °C   |

## Capacitance (T<sub>A</sub> = +25°C, V<sub>IN</sub> = 0V, f = 1.0 MHz)

| Description        | Symbol           | Limits |     | Unit |
|--------------------|------------------|--------|-----|------|
|                    |                  | Min    | Max |      |
| Input Capacitance  | C <sub>IN</sub>  |        | 40  | pF   |
| Output Capacitance | C <sub>OUT</sub> |        | 40  | pF   |

These parameters are guaranteed, but not tested.

**DC Characteristics** ( $V_{CC} = 5V$ )

| Parameter                 | Symbol         | Min   | Max  | Unit    |
|---------------------------|----------------|-------|------|---------|
| Input Leakage Current     | $I_{LI}^{(1)}$ | -10.0 | 10.0 | $\mu A$ |
| Output Leakage Current    | $I_{LO}^{(2)}$ | -10.0 | 10.0 | $\mu A$ |
| Output Low Voltage        | $V_{OL}^{(3)}$ |       | 0.4  | V       |
| Output High Voltage       | $V_{OH}^{(4)}$ | 2.4   |      | V       |
| Standby Supply Current    | $I_{SB}^{(5)}$ | 25ns  | 60   | mA      |
|                           |                | 35ns  | 50   |         |
|                           |                | 45ns  | 50   |         |
| Dynamic Operating Current | $I_{CC}^{(6)}$ | 25ns  | 150  | mA      |
|                           |                | 35ns  | 150  |         |
|                           |                | 45ns  | 150  |         |

**Notes:**

- (1)  $V_{CC} = \text{Max}$ ,  $V_{IO} = V_{CC}$  to GND.
- (2)  $V_{IO} = V_{CC}$  to GND,  $CE\# \geq V_{IH}$ ,  $OE\# \geq V_{IH}$ .
- (3)  $V_{CC} = \text{Min}$ ,  $I_{OL} = +8mA$ .
- (4)  $V_{CC} = \text{Min}$ ,  $I_{OH} = -4mA$ .
- (5)  $CE\# = V_{IH}$ ,  $OE\# = V_{IH}$ ,  $I_{OUT} = 0mA$ , Min Cycle Time.
- (6)  $V_{CC} = \text{Max}$ ,  $CE\# = V_{IL}$ ,  $OE\# = V_{IH}$ ,  $I_{OUT} = 0mA$ , Min Cycle Time

## AC Characteristics

### Write Cycle

| Parameter                       | Symbol  | 25ns | 35ns | 45ns | Limits | Unit |
|---------------------------------|---------|------|------|------|--------|------|
| Write Cycle Time                | TAVAV   | 25   | 35   | 45   | min    | ns   |
| Address Set-up Time             | TAVWL   | 0    | 0    | 0    | min    | ns   |
| Address Valid to End of Write   | TAVWH   | 20   | 25   | 30   | min    | ns   |
| Data Valid to End of Write      | TDVWH   | 15   | 20   | 25   | min    | ns   |
| Chip Enable Low to End of Write | TELWH   | 20   | 25   | 30   | min    | ns   |
| Write Pulse Width               | TWLWH   | 20   | 25   | 30   | min    | ns   |
| Address Hold from Write End     | TWHAX   | 0    | 0    | 0    | min    | ns   |
| Data Hold Time                  | TWHDX   | 0    | 0    | 0    | min    | ns   |
| Write Enable Low to High Z      | TWLQZ * | 15   | 20   | 25   | max    | ns   |
| Output Active from End of Write | TWHQX * | 5    | 5    | 5    | min    | ns   |

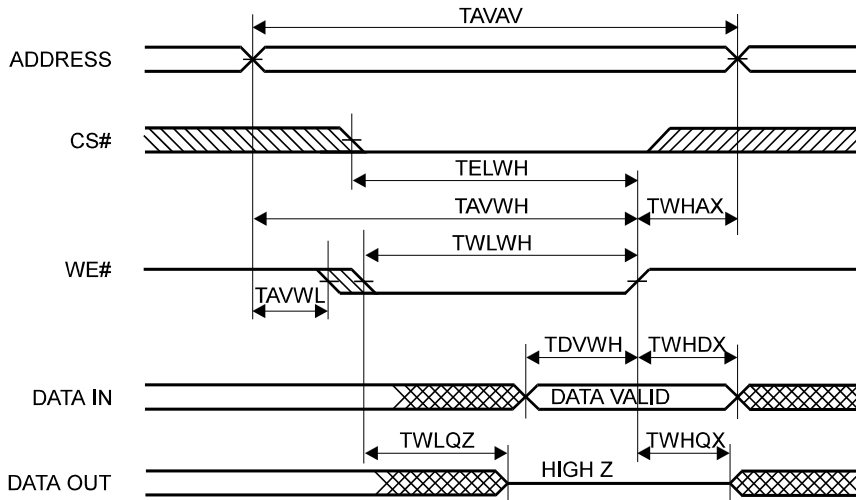
### Read Cycle

| Parameter                          | Symbol  | 25ns | 35ns | 45ns | Limits | Unit |
|------------------------------------|---------|------|------|------|--------|------|
| Read Cycle Time                    | TAVAV   | 25   | 35   | 45   | min    | ns   |
| Address Access Time                | TAVQV   | 25   | 35   | 45   | max    | ns   |
| Output Hold from Addr. Change      | TAVQX   | 5    | 5    | 5    | min    | ns   |
| Chip Enable Access Time            | TELQV   | 25   | 35   | 45   | max    | ns   |
| Output Enable to Output Valid      | TGLQV   | 20   | 25   | 35   | max    | ns   |
| Chip Enable to Output in Low Z     | TELQX * | 5    | 5    | 5    | min    | ns   |
| Chip Disable to Output in High Z   | TEHQZ * | 15   | 15   | 20   | max    | ns   |
| Output Enable to Output in Low Z   | TGLQX * | 5    | 5    | 5    | min    | ns   |
| Output Disable to Output in High Z | TGHQZ * | 15   | 20   | 25   | max    | ns   |

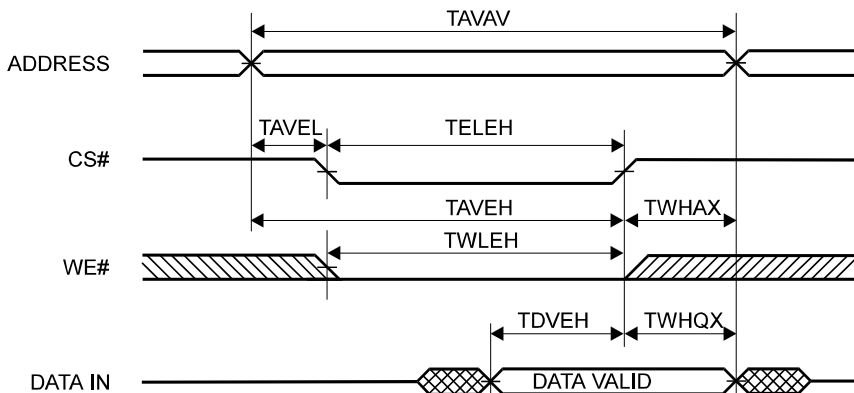
(\*) - Parameter is guaranteed, but not tested.

### Timing Waveforms of Write Cycle

#### Write Cycle 1: WE# Controlled (OE# = VIH)

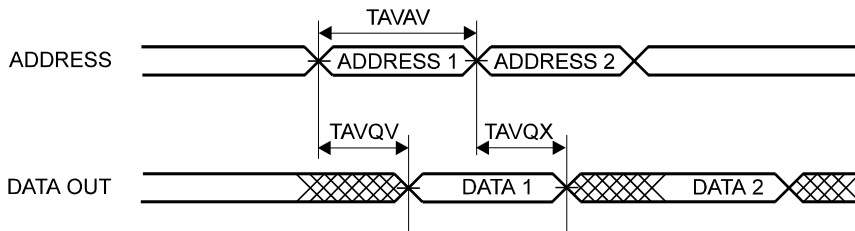


#### Write Cycle 2: CE# Controlled (OE# = VIH)

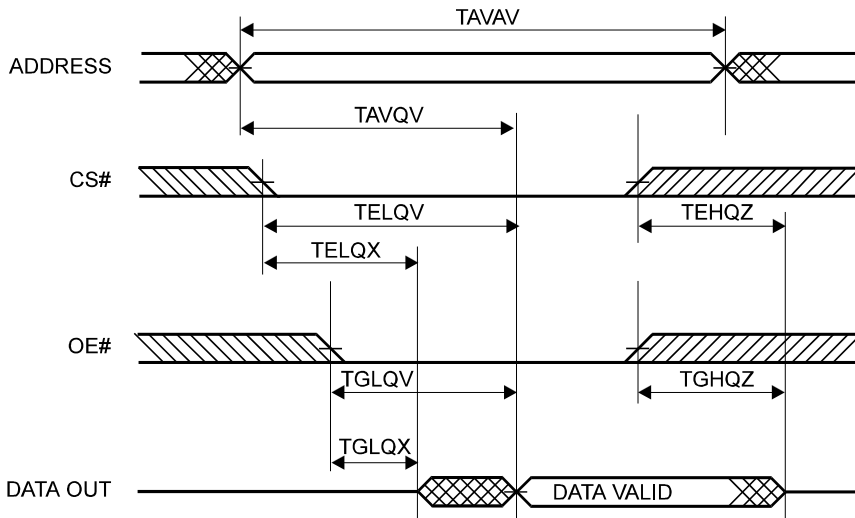


## Timing Waveforms of Read Cycle

### Read Cycle 1 (CS# = OE# = VIL, WE# = VIH)



### Read Cycle 2 (WE# = VIH)



## AC Test Conditions

| Item                          | Conditions                                  |
|-------------------------------|---|
| Input Pulse Levels            | GND to 3.0V                                 |
| Input Rise and Fall Times     | 5ns   |
| Input Timing Reference Level  | 1.5V  |
| Output Timing Reference Level | 1.5V  |
| Output Load:                  | 25ns to 70ns<br>85ns and up                 |
|                               | 1 TTL Load, CL=30pF<br>1 TTL Load, CL=100pF |

**Note:** For TWHQX, TWLQZ, TELQX, TEHQZ, TGLQX and TGHQZ CL = 5pF

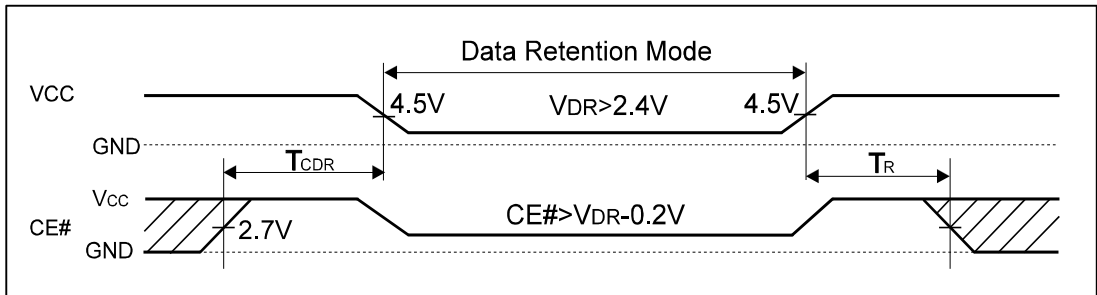
## Data Retention Characteristics (Over Operating Temp Range) For Low Power Version Only

Test Conditions: GND = 0V, CE# ≥ Vcc-0.2V, VIH ≥ Vcc - 0.2V, VIL ≤ 0.2V.

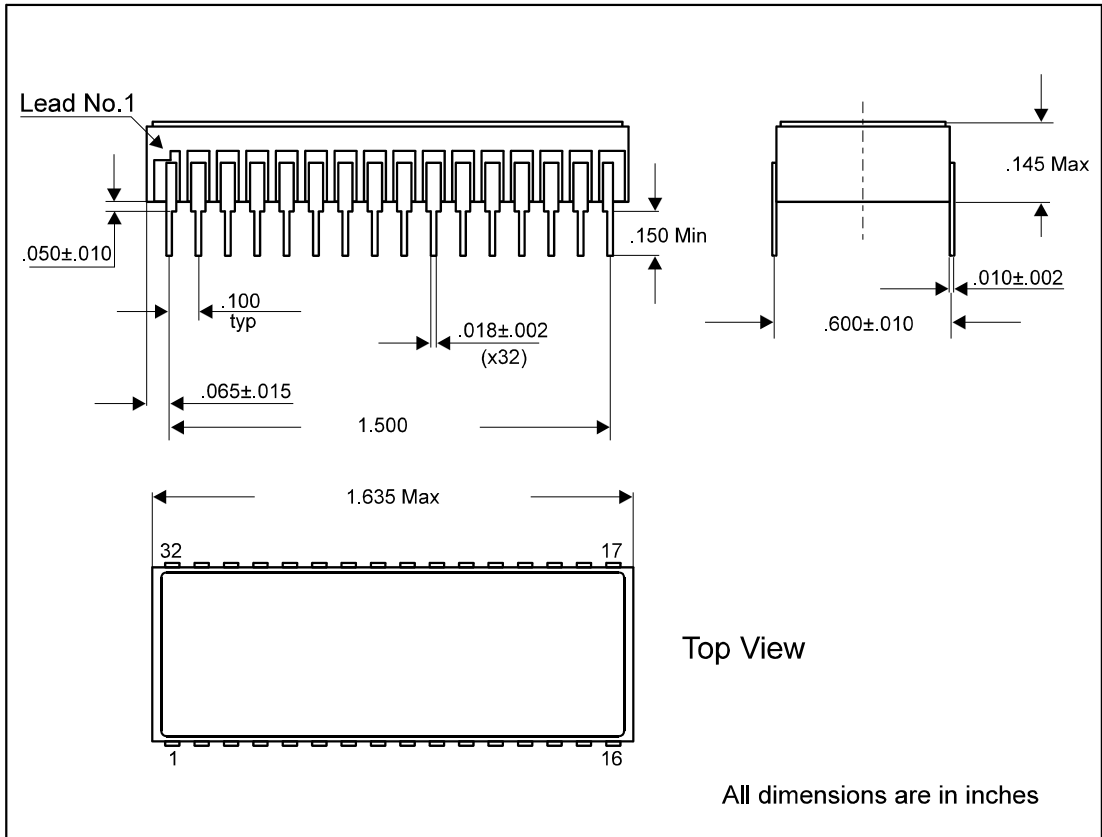
| Characteristic            | Symbol | Min                  | Typ. | Max  | Unit |
|---------------------------|--------|----------------------|------|------|------|
| VCC for Data Retention    | VDR    | 2                    |      |      | V    |
| D.R Quiescent Current     | ICDDR  |                      | 200  | 3000 | μA   |
| Chip Disable to D.R. Time | TCDR   | 0                    |      |      | nSec |
| Operation Recovery Time   | TR     | TAVAV <sup>(1)</sup> |      |      | nSec |

(1) TAVAV = Read Cycle Time

## Data Retention (CE# - Controlled)



**Outline Drawing for 32-Pin Ceramic DIP (D)**



**Ordering Information (Standard Military Screened Products\*)**

| <i>Model Number</i> | <i>Speed</i> | <i>Package</i> |
|---------------------|--------------|----------------|
| MES2568D25M         | 25ns         | CDIP32         |
| MES2568D25ML        | 25ns         | CDIP32         |
| MES2568D35M         | 35ns         | CDIP32         |
| MES2568D35ML        | 35ns         | CDIP32         |
| MES2568D45M         | 45ns         | CDIP32         |
| MES2568D45ML        | 45ns         | CDIP32         |

(\*) - Contact Elisra for additional designs

**Part Number Breakdown**

