

## 2Mbit, 256Kx8 CMOS S-RAM MODULE

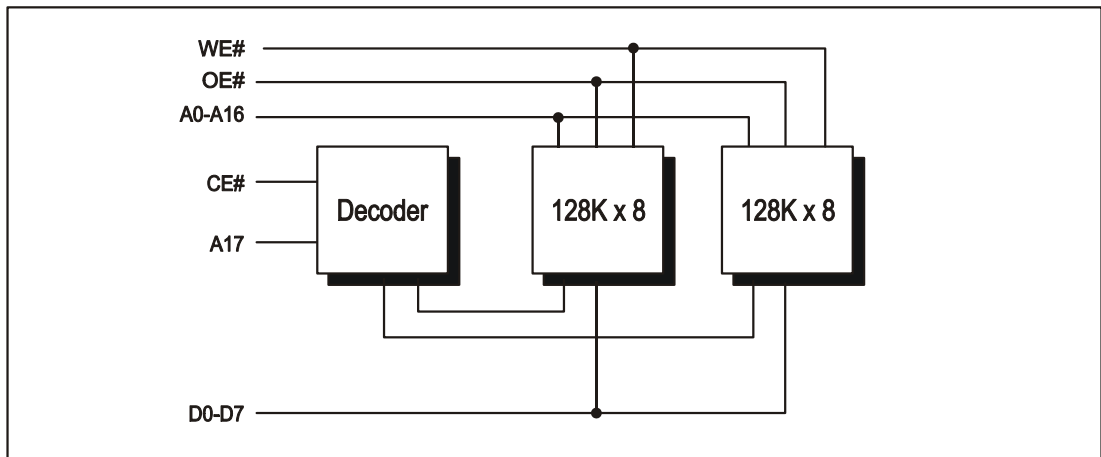
### Features

- Access Times: 55, 70, 85 and 100ns
- 32 Pin DIP, JEDEC Standard Pin Configuration
- Industrial and Military Screening
- Low Voltage Data Retention
- TTL Compatible Input/Output
- Fully Static, No Clocks
- Single 5V ( $\pm 10\%$ ) Power

### Product Description

The MES2568D is a Family of 2 Megabit Static Ram modules organized as 256Kx8. Each module is constructed from two 128Kx8 Static Rams. The 32-DIP package is a multilayered High Temperature cofired ceramic package designed for high speed and better ground bounce. These modules are available in 55 to 100ns versions.

### Block Diagram



### Pin Names

Pin Name	Pin Function
A0+A17	Address Inputs
DQ0+DQ7	Data Inputs/Outputs
CE#	Chip Enable
WE#	Write Enable
OE#	Output Enable
GND	Ground
Vcc	Power (+5V $\pm$ 10%)
NC	No Connection

### Truth Table (H=V<sub>IH</sub> L=V<sub>IL</sub> X=Don't Care)

OE#	WE#	CS#	I/O	Mode
X	X	H	Hi-Z	Standby
L	H	L	<b>DOUT</b>	Read
X	L	L	<b>DIN</b>	Write
H	H	L	Hi-Z	Out Disable

**Note:** # Symbol means Active Low Signal

### Pin Configuration (Top View)

1	● NC	Vcc ●	32
2	● A16	A15 ●	31
3	● A14	A17 ●	30
4	● A12	WE# ●	29
5	● A7	A13 ●	28
6	● A6	A8 ●	27
7	● A5	A9 ●	26
8	● A4	A11 ●	25
9	● A3	OE# ●	24
10	● A2	A10 ●	23
11	● A1	CE# ●	22
12	● A0	D7 ●	21
13	● D0	D6 ●	20
14	● D1	D5 ●	19
15	● D2	D4 ●	18
16	● GND	D3 ●	17

## Absolute Maximum Ratings

Item	Rating
Supply Voltage Relative to GND	-0.5V to +7.0V
Voltage on Any Pin Relative to GND	-0.5V to Vcc +0.5V
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

## Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	Vcc +0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temperature (Military)	T <sub>A</sub>	-55	+125	°C
Operating Temperature (Industrial)		-40	+85	°C

## Capacitance (T<sub>A</sub> = +25°C, V<sub>IN</sub> = 0V, f = 1.0 MHz)

Description	Symbol	Limits		Unit
		Min	Max	
Input Capacitance	C <sub>IN</sub>		40	pF
Output Capacitance	C <sub>OUT</sub>		40	pF

These parameters are guaranteed, but not tested.

**DC Characteristics** ( $V_{CC} = 5V$ )

Parameter	Symbol	Min	Max	Units	
Input Leakage Current	$I_{LI}^{(1)}$	-10.0	10.0	$\mu A$	
Output Leakage Current	$I_{LO}^{(2)}$	-10.0	10.0	$\mu A$	
Output Low Voltage	$V_{OL}^{(3)}$		0.4	V	
Output High Voltage	$V_{OH}^{(4)}$	2.4		V	
Standby Supply Current	$I_{SB}^{(5)}$	55ns		30	mA
		70ns		30	
		85ns		4	
		100ns		4	
Dynamic Operating Current	$I_{CC}^{(6)}$	55ns		90	mA
		70ns		90	
		85ns		70	
		100ns		60	

**Notes:**

- (1)  $V_{CC} = \text{Max}$ ,  $V_{I/O} = V_{CC}$  to GND.
- (2)  $V_{I/O} = V_{CC}$  to GND,  $CE\# \geq V_{IH}$ ,  $OE\# \geq V_{IH}$ .
- (3)  $V_{CC} = \text{Min}$ ,  $I_{OL} = +2.1\text{mA}$ .
- (4)  $V_{CC} = \text{Min}$ ,  $I_{OH} = -1.0\text{mA}$ .
- (5)  $CE\# = V_{IH}$ ,  $OE\# = V_{IH}$ ,  $I_{OUT} = 0\text{mA}$ , Min Cycle Time.
- (6)  $V_{CC} = \text{Max}$ ,  $CE\# = V_{IL}$ ,  $OE\# = V_{IH}$ ,  $I_{OUT} = 0\text{mA}$ , Min Cycle Time.

## AC Characteristics

### Write Cycle

Parameter	Symbol	55ns	70ns	85ns	100ns	Limits	Units
Write Cycle Time	TAVAV	55	70	85	100	min	ns
Address Set-up Time	TAVWL	0	0	0	0	min	ns
Address Valid to End of Write	TAVWH	50	50	70	75	min	ns
Data Valid to End of Write	TDVWH	25	30	40	45	min	ns
Chip Select Low to End of Write	TELWH	40	60	75	85	min	ns
Write Pulse Width	TWLWH	40	50	60	70	min	ns
Address Hold from Write End	TWHAX	0	0	0	0	min	ns
Data Hold Time	TWHDX	0	0	0	0	min	ns
Write Enable Low to High Z	TWLQZ *	25	25	30	35	max	ns
Output Active from End of Write	TWHQX *	5	10	10	10	min	ns

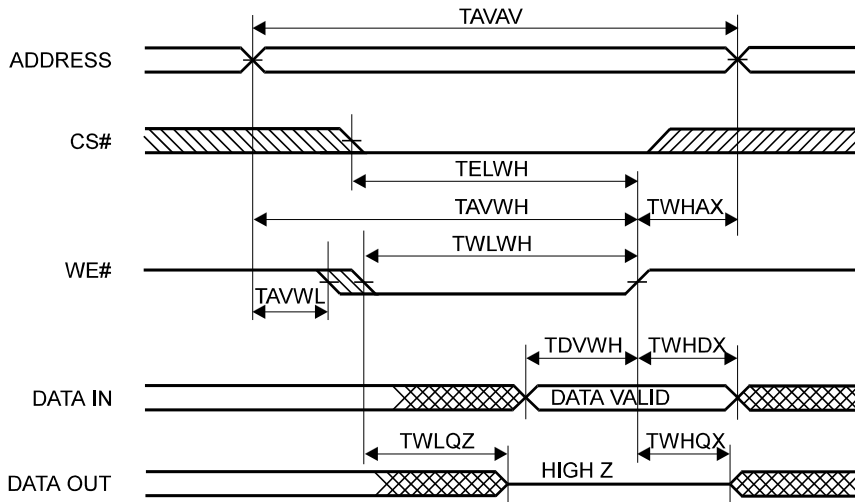
### Read Cycle

Parameter	Symbol	55ns	70ns	85ns	100ns	Limits	Units
Read Cycle Time	TAVAV	55	70	85	100	min	ns
Address Access Time	TAVQV	55	70	85	100	max	ns
Output Hold from Addr. Change	TAVQX	5	5	15	15	min	ns
Chip Enable Access Time	TELQV	55	70	85	100	max	ns
Output Enable to Output Valid	TGLQV	40	50	55	60	max	ns
Chip Enable to Output in Low Z	TELQX *	5	5	10	10	min	ns
Chip Disable to Output in High Z	TEHQZ *	30	35	40	45	max	ns
Output Enable to Output in Low Z	TGLQX *	5	5	5	5	min	ns
Output Disable to Output in High Z	TGHQZ *	30	30	40	40	max	ns

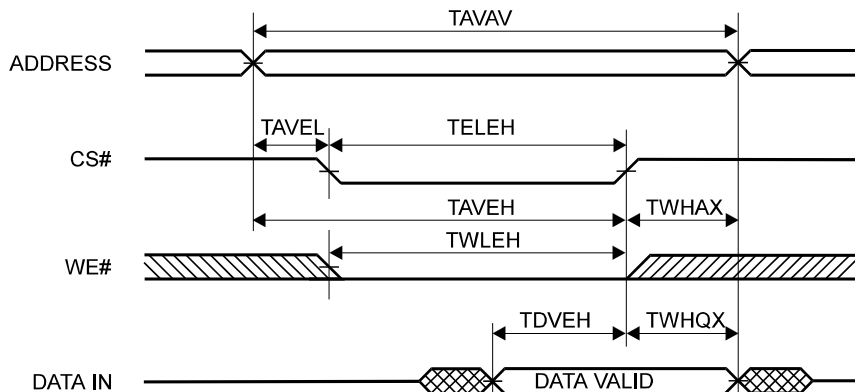
(\*) - Parameter is guaranteed, but not tested.

## Timing Waveforms of Write Cycle

### Write Cycle 1: WE# Controlled (OE# = VIH)

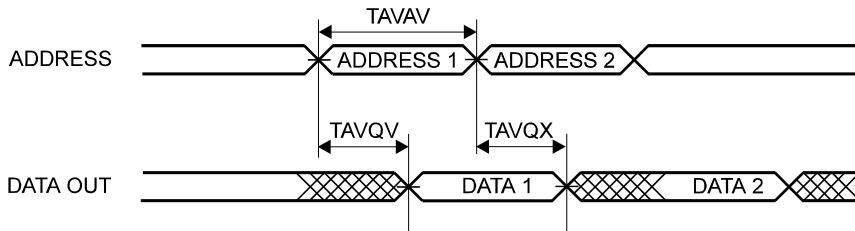


### Write Cycle 2: CE# Controlled (OE# = VIH)

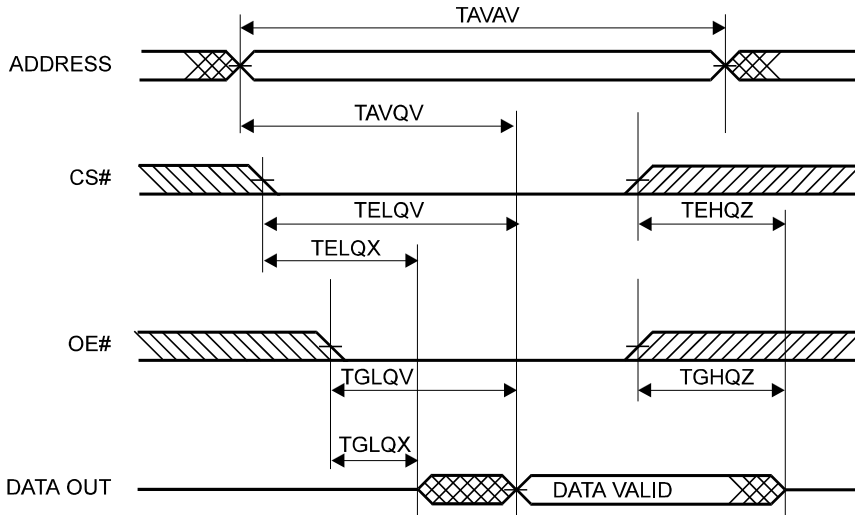


## Timing Waveforms of Read Cycle

### Read Cycle 1 (CS# = OE# = VIL, WE# = VIH)



### Read Cycle 2 (WE# = VIH)



### AC Test Conditions

Item	Conditions
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load:	25ns to 70ns 85ns and up
	1 TTL Load, CL=30pF 1 TTL Load, CL=100pF

**Note:** For TWHQX, TWLQZ, TELQX, TEHQZ, TGLQX and TGHQZ CL = 5pF

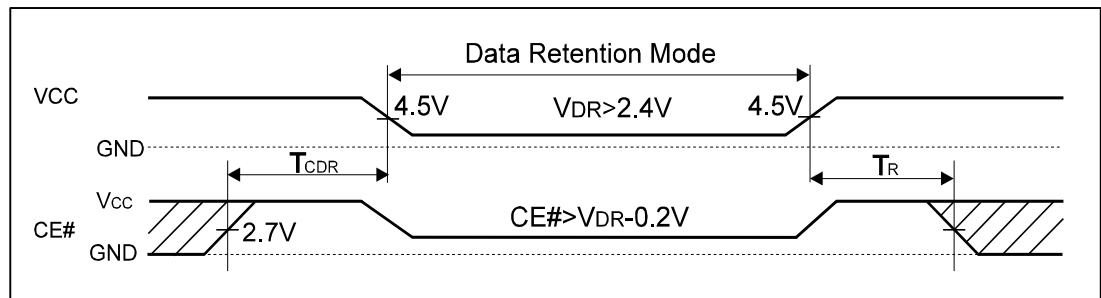
### Data Retention Characteristics (Over Operating Temp Range)

Test Conditions: GND = 0V, CE# ≥ Vcc-0.2V, VIH ≥ Vcc - 0.2V, VIL ≤ 0.2V.

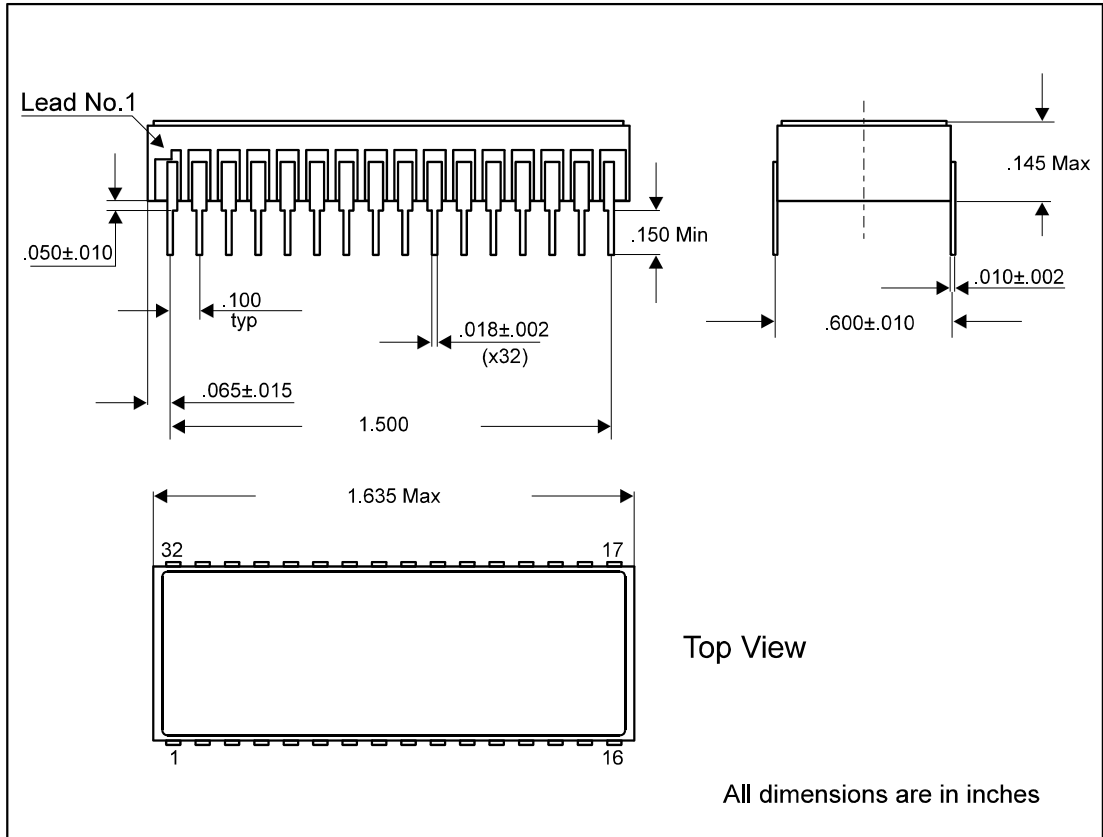
Characteristic	Symbol	Min	Typ.	Max	Unit
VCC for Data Retention	VDR	2			V
D.R Quiescent Current	ICCDR		20	1000 <sup>(2)</sup>	μA
Chip Disable to D.R. Time	TCDR	0			ns
Operation Recovery Time	TR	TAVAV <sup>(1)</sup>			ns

(1) TAVAV = Read Cycle Time      (2) 2000 μA (Max) for 55ns

### Data Retention (CE# - Controlled)



**Outline Drawing for 32-Pin Ceramic DIP (D)**



**Ordering Information (Standard Military Screened Products\*)**

<b>Model Number</b>	<b>Speed</b>	<b>Package</b>
MES2568D55M	55ns	CDIP32
MES2568D70M	70ns	CDIP32
MES2568D85M	85ns	CDIP32
MES2568D100M	100ns	CDIP32

(\*) - Contact Elisra for additional designs

**Part Number Breakdown**

