

## 128KX8 CMOS S-RAM (Monolithic)

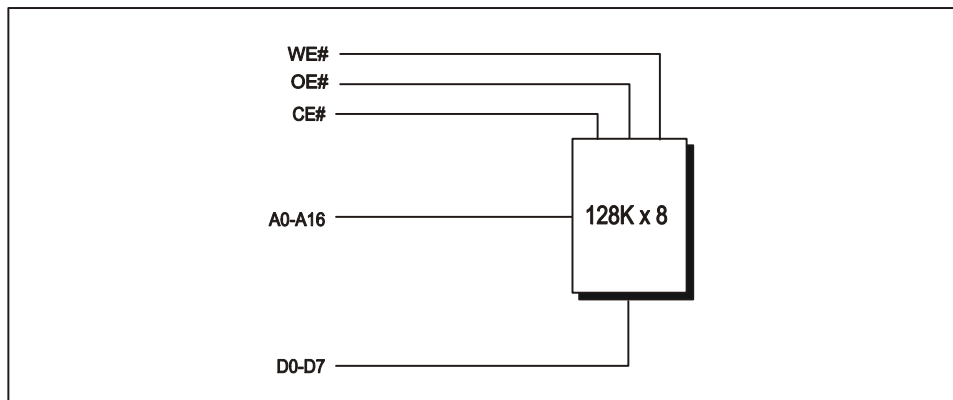
### Features

- Access Times: 55, 70, 85 and 100ns
- Package Options:
  - 32-Pin Ceramic DIP
  - 32-Lead Ceramic SOJ
- JEDEC Approved Pinout
- Industrial and Military Screening
- TTL Compatible Input/Output
- Single 5V ( $\pm 10\%$ ) Power
- Low Voltage Data Retention

### Product Description

The MES1288 is a Monolithic 1 Megabit Static Ram Devices organized as 128KX8. Each Device is constructed from one 128KX8 Static Ram Die, packed in a multilayered High Temperature cofired ceramic package, designed for high speed and better ground bounce. These Modules are available in 55 to 100ns versions.

### Block Diagram



### Pin Names

Pin Name	Pin Function
A0÷A16	Address Inputs
DQ0÷DQ7	Data Inputs/Outputs
CS#	Chip Select
WE#	Write Enable
OE#	Output Enable
GND	Ground
Vcc	Power (+5V ±10%)
NC	No Connection

### Truth Table (H=V<sub>IH</sub> L=V<sub>IL</sub> X=Don't Care)

OE#	WE#	CS#	I/O	Mode
X	X	H	Hi-Z	Standby
L	H	L	Dout	Read
X	L	L	Din	Write
H	H	L	Hi-Z	Out Disable

Note: # Symbol means Active Low Signal

### Pin Configuration (Top View)

1	● NC	VCC ●	32
2	● A16	A15 ●	31
3	● A14	NC ●	30
4	● A12	WE# ●	29
5	● A7	A13 ●	28
6	● A6	A8 ●	27
7	● A5	A9 ●	26
8	● A4	A11 ●	25
9	● A3	OE# ●	24
10	● A2	A10 ●	23
11	● A1	CS# ●	22
12	● A0	D7 ●	21
13	● D0	D6 ●	20
14	● D1	D5 ●	19
15	● D2	D4 ●	18
16	● GND	D3 ●	17

## Absolute Maximum Ratings

Item	Rating
Supply Voltage Relative to GND	-0.5V to +7.0V
Voltage on Any Pin Relative to GND	-0.5V to $V_{CC} + 0.5V$
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

## Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.5	V
Input High Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.5	+0.8	V
Operating Temperature (Military)	$T_A$	-55	+125	°C
Operating Temperature (Industrial)		-40	+85	°C

## Capacitance ( $T_A = +25^\circ\text{C}$ , $V_{IN} = 0V$ , $f = 1.0\text{ MHz}$ )

Description	Symbol	Limits		Unit
		Min	Max	
Input Capacitance	$C_{IN}$		30	pF
Output Capacitance	$C_{OUT}$		30	pF

These parameters are guaranteed, but not tested.

**DC Characteristics** ( $V_{CC} = 5V$ )

Parameter	Symbol	Min	Max	Units	
Input Leakage Current	$I_{LI}^{(1)}$	-2	2	$\mu A$	
Output Leakage Current	$I_{LO}^{(2)}$	-2	2	$\mu A$	
Output Low Voltage	$V_{OL}^{(3)}$		0.4	V	
Output High Voltage	$V_{OH}^{(4)}$	2.4		V	
Standby Supply Current (TTL levels)	$I_{SB}^{(5)}$	55 ns		3	mA
		70 ns		3	
		85 ns		3	
		100 ns		3	
Dynamic Operating Current	$I_{CC}^{(6)}$	55 ns		60	mA
		70 ns		55	
		85 ns		50	
		100 ns		50	

**Notes:**

- (1)  $V_{CC} = \text{Max}$ ,  $V_{I/O} = V_{CC}$  to GND.
- (2)  $V_{I/O} = V_{CC}$  to GND,  $CS\# \geq V_{IH}$ ,  $OE\# \geq V_{IH}$ .
- (3)  $V_{CC} = \text{Min}$ ,  $I_{OL} = +2.1\text{mA}$ .
- (4)  $V_{CC} = \text{Min}$ ,  $I_{OH} = -1.0\text{mA}$ .
- (5)  $CS\# = V_{IH}$ ,  $OE\# = V_{IH}$ ,  $I_{OUT} = 0\text{mA}$ , Min Cycle Time.
- (6)  $V_{CC} = \text{Max}$ ,  $CS\# = V_{IL}$ ,  $OE\# = V_{IH}$ ,  $I_{OUT} = 0\text{mA}$ , Min Cycle Time.

## AC Characteristics

### Write Cycle

Parameter	Symbol	55ns	70ns	85ns	100ns	Limits	Units
Write Cycle Time	TAVAV	55	70	85	100	min	ns
Address Set-up Time	TAVWL	0	0	0	0	min	ns
Address Valid to End of Write	TAVWH	45	60	70	90	min	ns
Data Valid to End of Write	TDVWH	25	30	35	40	min	ns
Chip Select Low to End of Write	TELWH	45	60	70	90	min	ns
Write Pulse Width	TWLWH	40	45	50	55	min	ns
Address Hold from Write End	TWHAX	0	0	0	0	min	ns
Data Hold Time	TWHDX	0	0	0	0	min	ns
Write Enable Low to High Z	TWLQZ *	20	30	30	40	max	ns
Output Active from End of Write	TWHQX *	5	10	10	10	min	ns

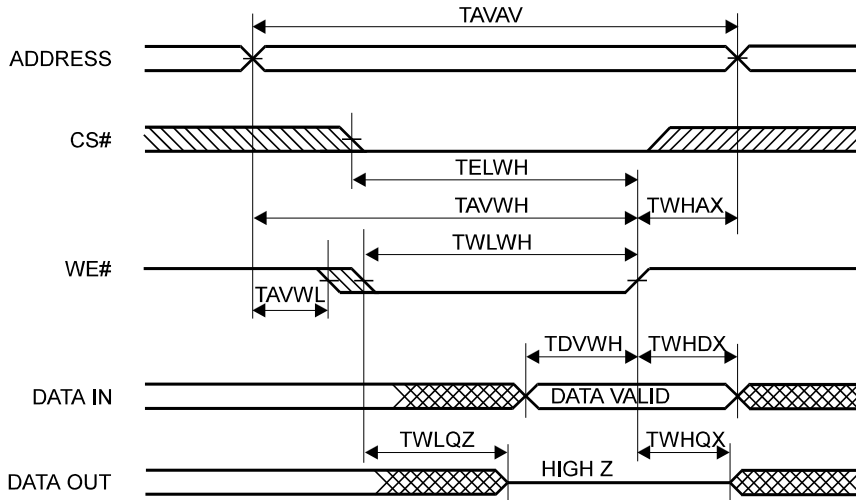
### Read Cycle

Parameter	Symbol	55ns	70ns	85ns	100ns	Limits	Unit
Read Cycle Time	TAVAV	55	70	85	100	min	ns
Address Access Time	TAVQV	55	70	85	100	max	ns
Output Hold from Addr. Change	TAVQX	5	5	15	15	min	ns
Chip Enable Access Time	TELQV	55	70	85	100	max	ns
Output Enable to Output Valid	TGLQV	30	35	40	50	max	ns
Chip Enable to Output in Low Z	TELQX *	5	5	5	5	min	ns
Chip Disable to Output in High Z	TEHQZ *	25	30	35	40	max	ns
Output Enable to Output in Low Z	TGLQX *	5	5	5	5	min	ns
Output Disable to Output in High Z	TGHQZ *	25	25	35	40	max	ns

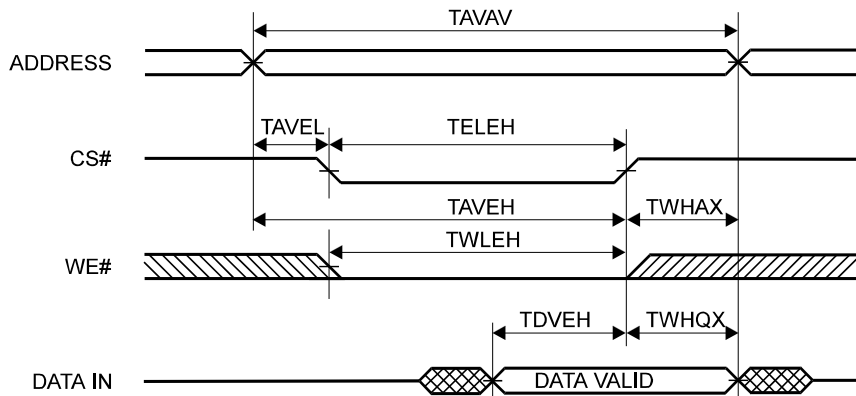
(\*) - Parameter is guaranteed, but not tested.

### Timing Waveforms of Write Cycle

#### Write Cycle 1: WE# Controlled (OE# = VIH)

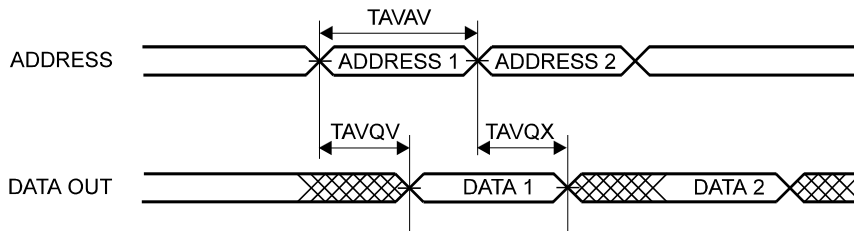


#### Write Cycle 2: CE# Controlled (OE# = VIH)

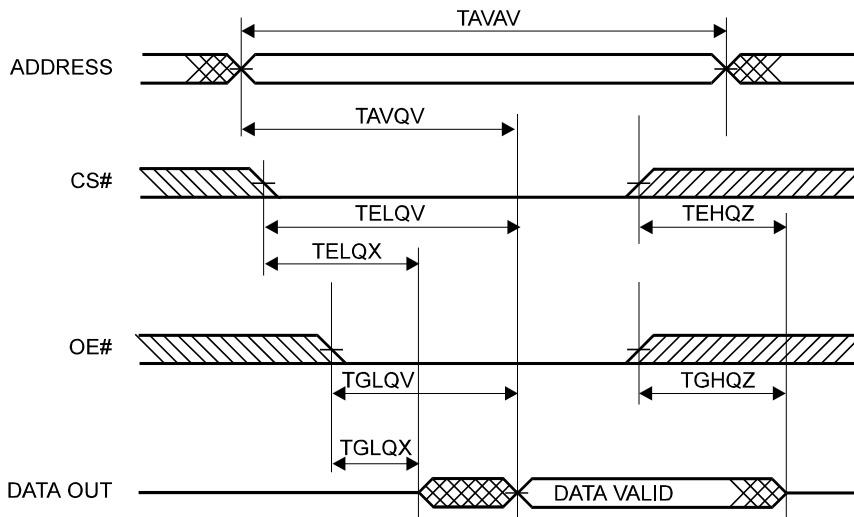


## Timing Waveforms of Read Cycle

### Read Cycle 1 (CS# = OE# = VIL, WE# = VIH)



### Read Cycle 2 (WE# = VIH)



## AC Test Conditions

Item	Conditions
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load:	25ns to 70ns 85ns and up
	1 TTL Load, CL=30pF 1 TTL Load, CL=100pF

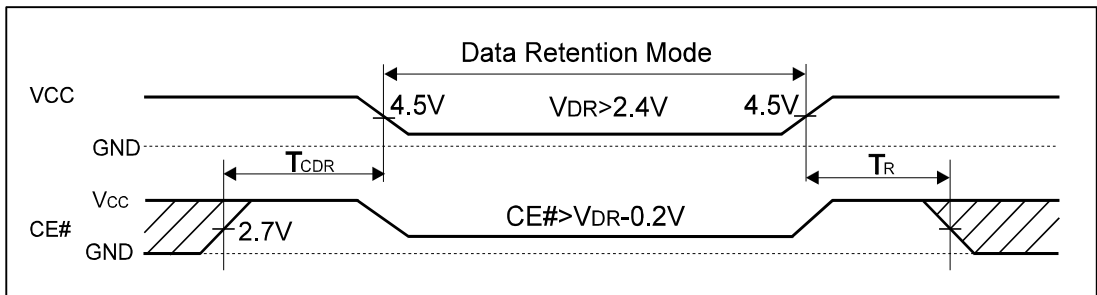
**Note:** For TWHQX, TWLQZ, TELQX, TEHQZ, TGLQX and TGHQZ CL = 5pF

## Data Retention Characteristics (Over Operating Temp Range)

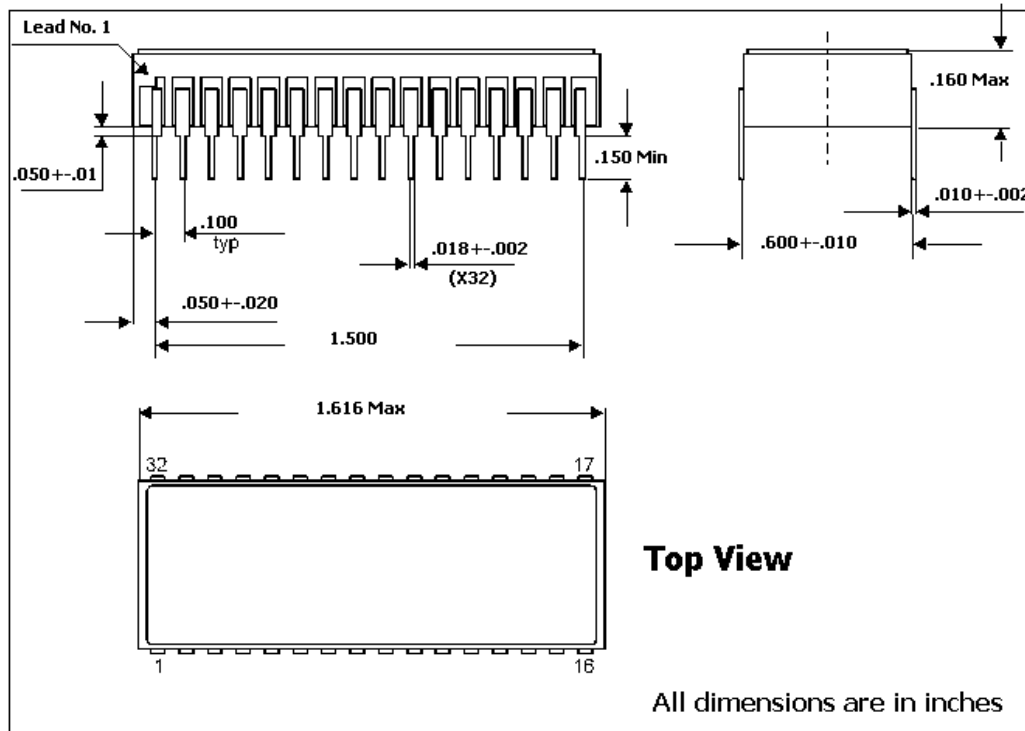
Test Conditions: GND = 0V, Vcc = 2V, CS# ≥ Vcc-0.2V, VIH ≥ Vcc - 0.2V, VIL ≤ 0.2V.

Characteristic	Symbol	Min	Typ.	Max	Unit
Vcc for Data Retention	VDR	2			V
D.R Quiescent Current	IccDR			500	μA
Chip Disable to D.R. Time	TCDR	0			ns
Operation Recovery Time	TR	TAVAV			ns

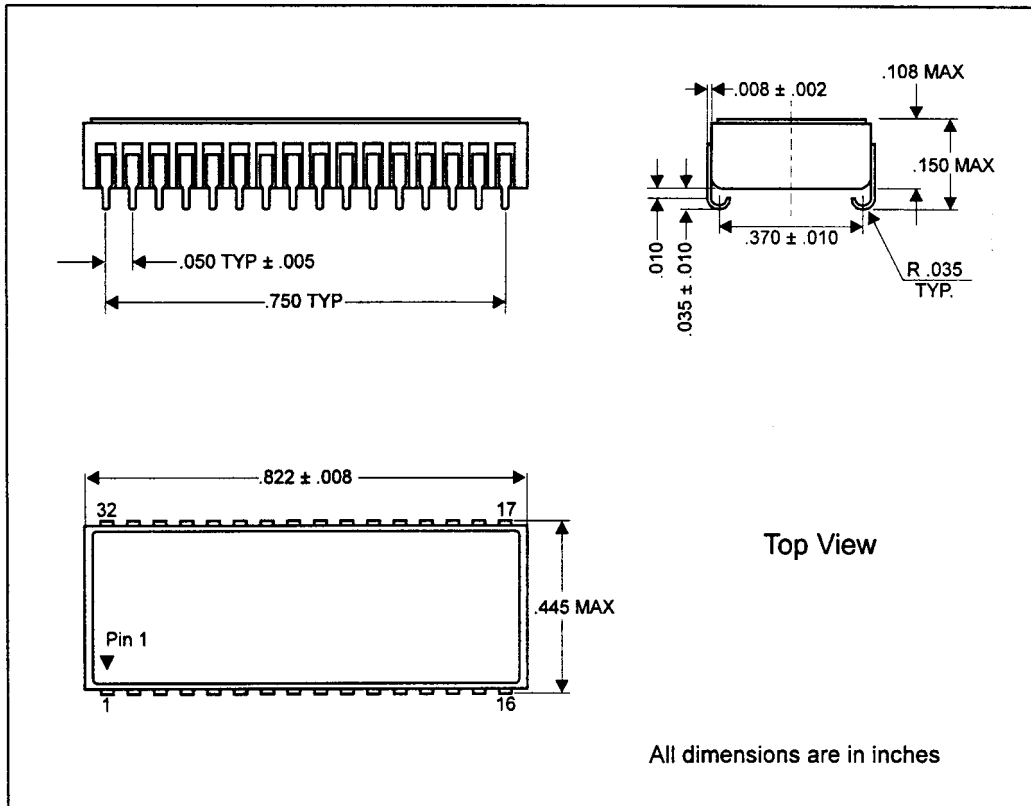
## Data Retention (CS# - Controlled)



**Outline Drawing for 32-Pin Ceramic DIP (D)**



**Outline Drawing for 32-Lead Ceramic SOJ (J1)**



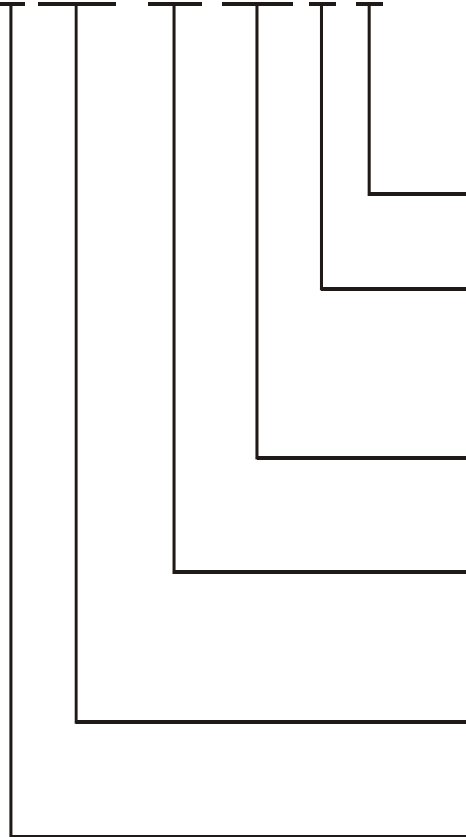
**Ordering Information (Standard Military Screened Products\*)**

<b><i>Model Number</i></b>	<b><i>Speed</i></b>	<b><i>Package</i></b>
<b>MES1288D55MN</b>	<b>55ns</b>	<b>CDIP32</b>
<b>MES1288D70MN</b>	<b>70ns</b>	<b>CDIP32</b>
<b>MES1288D85MN</b>	<b>85ns</b>	<b>CDIP32</b>
<b>MES1288D100MN</b>	<b>100ns</b>	<b>CDIP32</b>
<b>MES1288J155MN</b>	<b>55ns</b>	<b>CSOJ32</b>
<b>MES1288J170MN</b>	<b>70ns</b>	<b>CSOJ32</b>
<b>MES1288J185MN</b>	<b>85ns</b>	<b>CSOJ32</b>
<b>MES1288J1100MN</b>	<b>100ns</b>	<b>CSOJ32</b>

(\*) - Contact Elisra for additional designs

## Part Number Breakdown

**ME S 1288 XX XXX X N**



**Monolithic**

**Screening Options**

M = Military Full Screen

E = Extended Temp Range (-55°C to +125°C)

I = Industrial Grade (-40°C to +85°C)

**Speed Options**

Access Time (tAA) in ns

**Package**

D = Ceramic Dual In-Line

J1 = Ceramic SOJ

**Organization**

128K x 8

**Memory Type**

Static Ram